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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,712	ISLAM ET AL.	
	Examiner	Art Unit	
	ANGEL ROMAN	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 5, 6, 8-11, 14, 16, 17, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001.

Regarding claim 1, Seo et al. discloses a semiconductor device package (102, 106) comprising: a molding compound (18) forming at least a portion of a first package face (see figure 2B); a semiconductor device (4) at least partially covered by the molding compound (18), the semiconductor device (4) including a plurality of I/O pads (13); and a lead frame of electrically conductive material at least partially covered by the molding compound (18), the lead flame including a plurality of leads (12), each of the leads (12) including: an interposer having opposing first and second ends, the interposer being spaced apart from the first package face, a board connecting post extending from the interposer proximate the first end and terminating at the first package face, a support post spaced apart from the board connecting post, the support

post extending from the interposer proximate the second end and terminating at the first package face, and a bond site formed on a surface of the interposer opposite the support post, at least one of the I/O pads (13) being electrically connected to the interposer at the bond site (see figures 2B and 4B).

Regarding claim 2, Seo et al. discloses the at least one of the I/O pads (13) being wire bonded or tape bonded to the bond site (see figure 4B).

Regarding claim 5, Seo et al. discloses the at least one of the I/O pads (13) being directly soldered to the bond site for forming a flip-chip type connection (see figure 2B).

Regarding claim 6, Seo et al. discloses the molding compound (18) forming at least a portion of a second package face adjacent to the first package face, and a side surface (12c) of the board connecting post adjacent an end surface of the board connecting post is visible at the second package face (see figure 2B).

Regarding claim 8, Seo et al. discloses each of the leads (12) being formed from a strip of material having a channel (12a) disposed across the strip (see figure 2B).

Regarding claim 9, Seo et al. discloses the channel (12a) being filled with the molding compound (18).

Regarding claim 10, Seo et al. discloses method of packaging a semiconductor device (4), the method comprising: forming a lead frame from electrically conductive material, the lead frame including a plurality of leads (12), each of the leads (12) including: an interposer having opposing first and second ends, a board connecting post extending from the interposer proximate the first end, the board connecting post having an end surface distal from the interposer, a support post spaced apart from the board connecting post and extending from the interposer proximate the second end, the support post having an end surface distal from the interposer, and a bond site formed on a surface of the interposer opposite the support post; supporting the end surfaces of the support post and the board connecting post (see figures 2B and 4B); and electrically connecting I/O pads (13) on the semiconductor device (4) to the bond sites while supporting the end surfaces of the support post and the board connecting post (see figure 2B); and covering at least a portion of the semiconductor device (4), and at least a portion of the lead flame with a molding compound (18) while supporting the end surfaces of the support post and the board connecting post (the supporting is implicitly disclosed since molding and contact bonding require physical support).

Regarding claim 11, Seo et al. discloses electrically connecting the I/O pads (13) to the bond sites including: wire bonding or tape bonding each I/O pad (13) to an associated bond site (see figure 4B).

Regarding claim 14, Seo et al. discloses electrically connecting the I/O pads (13) to the bond sites includes: directly electrically connecting the I/O pads (13) to the bond sites to form a flip- chip type connection (see figure 2B).

Regarding claim 16, Seo et al. discloses the molding compound (18) forming at least a portion of a first package face, and the end surfaces of the support post and the bond connecting post are coplanar with the first package face (see figure 4B).

Regarding claim 17, Seo et al. discloses the molding compound (18) forming at least a portion of a second package face adjacent to the first package face, and a side surface (12c) of the board connecting post adjacent an end surface of the board connecting post is visible at the second package face (see figure 2B).

Regarding claim 19, Seo et al. discloses forming a lead frame precursor from electrically conductive material, the lead frame precursor including a plurality of lead precursors, each of the lead precursors being a strip of the conductive material (see figure 4B); and disposing a channel (12a) across each of the lead precursors to form the plurality of leads (see figure 4B).

Regarding claim 20, Seo et al. discloses filling the channel (12a) in each lead with the molding compound (18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001.

Regarding claim 7, Seo et al. discloses a corner between the side surface of the board connecting post and the end surface of the board connecting post being removed to form a relief, the relief having a height of a groove 12a (see figure 2B) of. Seo et al. lacks disclosing a value between about 1 mils to about 2 mils for the groove's (12a) height. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select 1 mils to about 2 mils for the groove's (12a) height, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 18, Seo et al. discloses a corner between the side surface of the board connecting post and the end surface of the board connecting post being removed to form a relief, the relief having a height of a groove 12a (see figure 2B) of. Seo et al. lacks disclosing a value between about 1 mils to about 2 mils for the groove's (12a) height. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select 1 mils to about 2 mils for the groove's (12a) height, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001 in view of Ball U.S. Patent 6,299,057 dated 10/09/2001.

Regarding claim 15, Seo et al. implicitly discloses supporting the end surfaces of the support post and the board connecting post but lacks disclosing the support including adhering the end surfaces of the support post and the board connecting post to a surface. Ball disclosing supporting end surfaces of leads during a wire bonding process by adhering end surfaces of leads to support 14 (see figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to perform the wire bonding process in the primary reference of Seo et al. by adhering end surfaces of the support post and the board connecting post to a surface as disclosed in Ball in order to improve device reliability by preventing damage at bonding sites.

8. Claims 3, 4, 12, 13, 21-23 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001 in view of Sakamoto et al. U.S. Patent Application Publication 2001/0045625 A1 dated 11/29/2001.

Regarding claim 3, Seo et al. discloses the at least one of the I/O pads (13) being electrically connected to the interposer at the bond site by a wire (8) forming bond at the

I/O pad (13) and bond at the bond site (see figure 4B). Seo et al. lacks identifying the wire bonds as wedge bonds. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing cost and prevent damage to the semiconductor device since wedge bonding does not require application of heat.

Regarding claim 4, Seo et al. discloses the wire is made from aluminum or aluminum base (see column 6, lines 62-67).

Regarding claim 12, Seo et al. discloses bonding a wire (8) to the I/O pad (13), and bonding the wire (8) to the bond site (see figure 4B). Seo et al. lacks identifying the wire bonds as wedge bonds. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing cost and prevent damage to the semiconductor device since wedge bonding does not require application of heat.

Regarding claim 13, Seo et al. discloses the wire (8) being made of aluminum or aluminum base (see column 6, lines 62-67).

Regarding claim 21, Seo et al. discloses a semiconductor device package (106, 108) comprising: a molding compound (18) forming at least a portion of a first package face; a semiconductor device (2) at least partially covered by the molding compound (18); the semiconductor device (2) including a plurality of I/O pads (13); and a lead frame of electrically conductive material at least partially covered by the molding compound (18), the lead frame including a plurality of leads (12), each of the leads (12) including a bond site formed thereon, each bond site being electrically connected to an associated I/O pad (13) by a wire (8), the wire (8) forming a bond at the I/O pad (13) and a bond at the bond site (see figures 4B and 5B). Seo et al. lacks identifying the wire bonds as wedge bonds. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing cost and prevent damage to the semiconductor device since wedge bonding does not require application of heat.

Regarding claim 22, Seo et al. discloses the wire is made from aluminum or aluminum base (see column 6, lines 62-67).

Regarding claim 23, Seo et al. discloses each of the leads (12) further including: an interposer having opposing first and second ends, the interposer being spaced apart from the first package face, a board connecting post extending from the interposer proximate the first end and terminating at the first package face, a support post spaced apart from the board connecting post, the support post extending from the interposer proximate the second end and terminating at the first package face, the bond site being formed on a surface of the interposer opposite the support Post (see figures 4B and 5B).

Regarding claim 26, Seo et al. discloses a method of packaging a semiconductor device (2), the method comprising: forming a lead frame from electrically conductive material, the lead frame including a plurality of leads (12), each of the leads (12) including a bond site formed thereon; electrically connecting I/O pads (13) on the semiconductor device (2) to the bond sites, the electrically connecting including: bonding a wire (8) to the I/O pad (13), and bonding the wire (8) to the bond site; and covering at least a portion of the semiconductor device (2), and at least a portion of the lead flame with a molding compound (18). Seo et al. lacks identifying the wire bonds as wedge bonds. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing

cost and prevent damage to the semiconductor device since wedge bonding does not require application of heat.

Regarding claim 27, Seo et al. discloses the wire is made from aluminum or aluminum base (see column 6, lines 62-67).

Regarding claim 28, Seo et al. discloses each lead including an interposer having opposing first and second ends, a board connecting post extending from the interposer proximate the first end, the board connecting post having an end surface distal from the interposer, a support post spaced apart from the board connecting post and extending from the interposer proximate the second end, the support post having an end surface distal from the interposer, the bond site being formed on a surface of the interposer opposite the support post, the support post supporting the bond site during the bonding of the wire (8) to the bond site (see figures 4B and 5B).). Seo et al. lacks identifying the wire bonds as wedge bonds. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing cost and prevent damage to the semiconductor device since wedge bonding does not require application of heat.

Regarding claim 29, Seo et al. discloses bonding the wires (8) but lacks disclosing bonding by wedge bonding including ultrasonic bonding. Sakamoto et al. discloses a method of packaging a semiconductor device wherein a chip is wire bonded to a lead using ultrasonic wedge bonding (see paragraph [0170]). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to used ultrasonic wedge bonding to bond the wires in the primary reference of Seo et al. as disclosed in Sakamoto et al. in order to reduce processing cost and prevent damage to the semiconductor device since ultrasonic wedge bonding does not require application of heat.

9. Claims 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001 in view of Sakamoto et al. U.S. Patent Application Publication 2001/0045625 A1 dated 11/29/2001 as applied to claims 21 and 26 above, and further in view of Lin U.S. Patent 6,238,952 B1 dated 05/29/2001.

Regarding claim 24, Seo et al. as modified by Sakamoto et al. discloses the lead frame (302) with separated the leads (12). Seo et al. as modified by Sakamoto et al. lacks disclosing an etching process to separate the leads from the lead frame after the molding compound is applied to the lead frame. Lin discloses an etching process to separate leads from a lead frame after a molding compound is applied to the lead frame (see figures 7-12). It would have been obvious to a person having ordinary skills in the

art at the time the invention was made to separate the leads from a lead frame in the primary reference of Seo et al. as modified by Sakamoto et al. by etching a lead frame after an encapsulation process as disclosed in Lin in order to improve device reliability by performing the wire bonding process before separating the leads from the lead frame.

Regarding claim 32, Seo et al. as modified by Sakamoto et al. discloses electrically connecting the I/O pads (13) on the semiconductor device (2) to the bond sites and a lead frame (302) with separated the leads (12). Seo et al. as modified by Sakamoto et al. lacks disclosing an etching process to separate the leads from the lead frame after electrically connecting the I/O pads (13) on the semiconductor device (2) to the bond sites and after the molding compound is applied to the lead frame. Lin discloses an etching process to separate leads from a lead frame after electrically connecting the I/O pads on a semiconductor device to bond sites and after a molding compound is applied to the lead frame (see figures 7-12). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to separate the leads from a lead frame in the primary reference of Seo et al. as modified by Sakamoto et al. by etching a lead frame after electrically connecting the I/O pads on a semiconductor device to bond sites and after an encapsulation process as disclosed in Lin in order to improve device reliability by performing the wire bonding process before separating the leads from the lead frame.

10. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001 in view of Sakamoto et al. U.S. Patent Application Publication 2001/0045625 A1 dated 11/29/2001 as applied to claim 26 above, and further in view of Ball U.S. Patent 6,299,057 dated 10/09/2001.

Regarding claim 30, Seo et al. as modified by Sakamoto et al. discloses wedge bonding the wires but lacks disclosing thermosonic bonding to perform the wedge bonding process. Ball discloses thermosonic bonding to bond semiconductor wires (see column 2, lines 8-20). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to use thermosonic bonding to bond the wires in the primary reference of Seo et al. as modified by Sakamoto et al. as disclosed in Ball in order improve mechanical strength of at the bonding site cause by the increase temperature effects.

Regarding claim 31, Seo et al. as modified by Sakamoto et al. discloses the wire (8) being bonded to the I/O pad (13) but lacks disclosing bonding the wire to the pad (13) before the wire (8) is bonded to the bond site. Ball discloses bonding a wire to a semiconductor connecting pad before bonding the wire to a bond site on a lead (see figure 1). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to bond the wire to a semiconductor connecting pad before bonding the wire to a bond site on a lead in the primary reference of Seo et al. as

modified by Sakamoto et al. as disclose in Ball in order to establish an electrical connection between the device and the lead.

11. Claims 25 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. U.S. Patent 6,759,737 B2 filed 03/23/2001 in view of Sakamoto et al. U.S. Patent Application Publication 2001/0045625 A1 dated 11/29/2001 as applied to claims 21 and 26 above, and further in view of Aoki U.S. Patent 5,263,246 dated 11/23/1993.

Regarding claim 25, Seo et al. as modified by Sakamoto et al. discloses wedge wire bonding wherein a portion of the wire is extending between the I/O pad (13) and the bond site but lacks disclosing the wire having a wedge width between about 1.2 to about 1.5 times a diameter of the wire. Aoki discloses a wire having a wedge width between about 1.2 to about 1.5 times a diameter of the wire (see column 2, lines 25-67). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to bond the wire to form a wedge width between about 1.2 to about 1.5 times a diameter of the wire in the primary reference of Seo et al. as modified by Sakamoto et al. as disclosed in Aoki in order to improve chip performance (see Aoki column 1, lines 50-55).

Regarding claim 33, Seo et al. as modified by Sakamoto et al. discloses wedge wire bonding wherein a portion of the wire is extending between the I/O pad (13) and

the bond site but lacks disclosing the wire having a wedge width between about 1.2 to about 1.5 times a diameter of the wire. Aoki discloses a wire having a wedge width between about 1.2 to about 1.5 times a diameter of the wire (see column 2, lines 25-67). It would have been obvious to a person having ordinary skills in the art at the time the invention was made to bond the wire to form a wedge width between about 1.2 to about 1.5 times a diameter of the wire in the primary reference of Seo et al. as modified by Sakamoto et al. as disclosed in Aoki in order to improve chip performance (see Aoki column 1, lines 50-55).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Noquil et al., Ahn et al., Fan et al., Pedron et al., Diot, Yamada et al. and Glenn et al disclosed related packages and methods of forming leadless semiconductor packages.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANGEL ROMAN whose telephone number is (571)272-6369. The examiner can normally be reached on IFP Mo-Fr 6am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. R./
Examiner, Art Unit 2812
September 16, 2008

/Alexander G. Ghyka/
Primary Examiner, Art Unit 2812